What Is Claimed Is:

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- 1. A reset pulse generator for a CPU, which generating
 2 an oscillating disable signal after initialization, comprising:
 3 an oscillating circuit coupled to the CPU to output a
 4 sequence of reset pulses to the CPU; and
 5 an oscillating disable circuit coupled to the oscillating
 6 circuit for disabling the oscillating circuit and
- The reset pulse generator as claimed in claim 1,
 wherein the oscillating circuit comprises:

oscillating disable signal is received.

initiating normal mode CPU operation when the

- a Schmitt trigger having an input terminal and an output terminal;
 - a resistor coupled between the input terminal and the output terminal; and
- a capacitor coupled to the input terminal and a ground level.
- 3. The reset pulse generator as claimed in claim 1, wherein the oscillating disable circuit is a switch turned on by the oscillating disable signal to stop oscillation of the oscillating circuit.
- 4. The reset pulse generator as claimed in claim 1, further comprising a manual switch to generate a start signal to enable the oscillating circuit.
- 5. The reset pulse generator as claimed in claim 1,
 wherein the start signal is generated during power on.

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- A reset pulse generator, comprising: 1 2 a CPU for generating an oscillating disable signal after 3 initialization: 4 an oscillating circuit coupled to the CPU to output a sequence of reset pulses to the CPU; and 5 an oscillating disable circuit coupled to the oscillating circuit for disabling the oscillating circuit and 7 initiating normal mode CPU operation when the 8 oscillating disable signal is received. 9 1 The reset pulse generator as claimed in claim 6, wherein the oscillating circuit comprises: 2 3 a Schmitt trigger having an input terminal and an output 4 terminal; a resistor coupled between the input terminal and the 5 output terminal; and 6 7 a capacitor coupled to the input terminal and a ground level. 8 1 The reset pulse generator as claimed in claim 6, wherein the oscillating disable circuit is a switch turned on 2 3 by the oscillating disable signal to stop oscillation of the oscillating circuit. 4 1 9. The reset pulse generator as claimed in claim 6, further comprising a manual switch to generate a start signal 2
 - 10. The reset pulse generator as claimed in claim 6, wherein the start signal is generated during power on.

to enable the oscillating circuit.